In the Drawings

Please replace Figure 1 with the attached replacement sheet of Figure 1. The arrow has been added to the line coupling return stage 152 and BPU 126, as the Examiner suggested.

Please replace Figure 2 with the attached replacement sheet of Figure 2. The reference sign "4N" has been replaced with the reference sign "3N", as the Examiner suggested.

Please replace Figure 3 with the attached replacement sheet of Figure 3. The reference signs 340 and 360 have been added to correspond with the Specification.

Please replace Figure 4 with the attached replacement sheet of Figure 4. The reference sign 2 has been inserted at bus 436, as the Examiner suggested.

Please replace Figure 5 with the attached replacement sheet of Figure 5. The reference signs 20 and 39 have been added to correspond with the Specification.

REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-24 are pending. Claims 1, 2, 4-13, 15-18, 20, 21, 23 and 24 have been rejected. Claims 3, 14, 19 and 22 have been objected to.

Claims 1, 6, 15, and 20 have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Applicants reserve the rights with respect to the applicability of the Doctrine of Equivalents.

Objections to the Specification

The title of the invention has been objected for not being descriptive.

The disclosure is objected to because of informalities.

The title has been amended to overcome the Examiner's objection.

Paragraph [0022] on page 10, line 19 has been amended to remove the redundant "may be", as the Examiner suggested.

Therefore, Applicant submits that the Examiner's title and specification objections have been overcome.

Drawing Objections

The drawings 3 and 5 have been objected to as failing to comply with 37 C.F.R. 1.84(p)(5), because they do not include the appropriate reference signs mentioned in the description.

The drawings of Figures 3 and 5 have been amended to overcome the Examiner's objections. The replacement drawing sheets for Figures 3 and 5 are submitted herewith.

The drawings of Figures 1-5 have been objected to as failing to comply with 37 C.F.R. 1.84(p)(5), because they include the references characters not mentioned in the description.

The present paragraphs [0012], [0017], [0025], [0026], [0032], and [0034] have been amended to include reference signs from Figures 1-5.

With respect to the objection to Figure 5, Applicant respectfully submits that reference numeral 30 is described in the present paragraph [0036] that reads as follows:

> **[0036]** Bus bridge 32 may permit data exchanges between system bus 6 and bus 16, which may in some embodiments be a industry standard architecture (ISA) bus or a peripheral component interconnect (PCI) bus. There may be various input/output I/O devices 14 on the bus 16, including in some embodiments low performance graphics controllers, video controllers, and networking controllers. Another bus bridge 18 may in some embodiments be used to permit data exchanges between bus 16 and bus 20. Bus 20 may in some embodiments be a small computer system interface (SCSI) bus, an integrated drive electronics (IDE) bus, or a universal serial bus (USB) bus. Additional I/O devices may be connected with bus 20. These may include keyboard and cursor control devices 22, including mice, audio I/O 24, communications devices 26, including modems and network interfaces, and data storage devices 28. Software code 30 may be stored on data storage device 28. In some embodiments, data storage device 28 may be a fixed magnetic disk, a floppy disk drive, an optical disk drive, a magneto-optical disk drive, a magnetic tape, or non-volatile memory including flash memory.

(emphasis added)

The drawings of Figures 1, 2, and 4 have been objected to because of minor informalities.

Figures 1, 2, and 4 have been amended to overcome the Examiner's objections. The replacement drawing sheets for Figures 1, 2, and 4 are submitted herewith.

Therefore, Applicant respectfully submits that the Examiner's objections to drawings of Figures 1-5 have been overcome.

Rejections Under 35 U.S.C. § 102

Claims 1-2 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,758,112 to Yeager, et al. ("Yeager").

Amended claim 1 reads as follows:

> A processor, comprising:
> a first register alias table including a first number of read ports to translate a first set of logical register addresses to physical register addresses; and
> a second register alias table including a second number of read ports to translate a second set of logical register addresses to physical register addresses, wherein said first number that includes at least one read port for each source operand for an instruction is greater than said second number. (emphasis added)

Applicant respectfully submits that these features as recited in amended claim 1 are not shown in Yeager.

Yeager discloses a processor that includes two register mapping tables 206 and 204 (Figure 3). More specifically, Yeager discloses

> Integer mapping table 206 has twelve read ports 354, as shown in FIG. 3, which map three logical register numbers (i.e., operands 368 and 370 and destination 372) for each integer instruction 366 (up to a maximum of four instructions in parallel). Each line 374 represents a five-bit logical register number (maximum of twelve lines for four instructions) and each line 376 represents a six-bit physical register number.
>
> Floating-point mapping table 204 has sixteen read ports 352, as shown in FIG. 3, which map four logical register numbers (i.e., operands 358, 360 and 362, and destination 364) for each floating-point instruction 356 (up to a maximum of four instructions in parallel). Each line 378 represents a five-bit logical register number (maximum of sixteen lines for four instructions) and each line 380 represents a six-bit physical register number. Instruction register 382 provides a total of four instructions (i.e., floating-point and/or integer) to the foregoing read ports during each cycle. As discussed below, each mapping table includes a number of mapping table cells (primary and redundant) and read and write decoders. (Yeager, col. 8, lines 47-67) (emphasis added)

Thus, Yeager merely discloses a mapping table that has one port for each source operand for one instruction, in contrast to a second register alias table including a second number of read ports to translate a second set of logical register addresses to physical register addresses, wherein the second number of the read ports is less that the first number that includes at least one read

port for each source operand for an instruction, as recited in amended claim 1. Because Yeager fails to disclose all limitations of amended claim 1, Applicant respectfully submits that amended claim 1 is not anticipated by Yeager under 35 U.S.C. § 102(b).

Given that claims 2-24 contain related limitations, Applicant respectfully submits that claims 2-24 are not anticipated by Yeager under 35 U.S.C. § 102(b).

Rejections Under 35 U.S.C. § 103

Claims 4-13, 15-18, 20-21 and 23-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yeager.

Yeager, in contrast to presently claimed invention, discloses redundant mapping tables for restoring the register renaming information in the event of a branch misprediction. As set forth above, Yeager merely discloses mapping tables that have one port for each source operand per instruction. It is respectfully submitted that Yeager fails to disclose, teach, or suggest a second register alias table including a second number of read ports to translate a second set of logical register addresses to physical register addresses, wherein said first number that includes at least one read port for each source operand for an instruction is greater than said second number, as recited in amended claim 1.

Therefore, Applicant respectfully submits that amended claim 1 is not obvious under 35 U.S.C. § 103(a) over Yeager.

Given that claims 4-13, 15-18, 20-21 and 23-24 contain related limitations, Applicant respectfully submits that claims 4-13, 15-18, 20-21 and 23-24 are not obvious under 35 U.S.C. § 103(a) over Yeager.

Allowable Subject Matter

Applicant notes with appreciation the Examiner's allowance of the claims 3, 14, 19 and 22, if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

At this time, however, Applicant elects not to place the limitations of the allowed claims into their corresponding independent claims because Applicant respectfully believes that the revised independent claims 1, 6, 15, and 20 are in condition for allowance.

Conclusion

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: September 20, 2006 By: _____

Tatiana Rossin
Reg.No.56,833

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(408) 720-8300